Claims

[c1] 1.A method of fabricating a capacitor, comprising:
forming a bottom electrode;
forming at least one lower surface expansion structure to the bottom electrode;
conformally depositing an insulator film to exposed portions of the bottom electrode and at least one lower surface expansion structure; and
forming a top electrode having a planar surface with at least one upper surface expansion structure separated from the at least one lower surface expansion structure by the insulator film.

[c2] 2.The method of claim 1, wherein forming a top electrode having a planar surface comprises planarizing a surface of the top electrode by a polishing process.

[c3] 3.The method of claim 1, wherein the bottom electrode is capacitively coupled to the top electrode substantially through sides of the at least one lower and upper surface expansion structures.

[c4] 4.The method of claim 1, further comprising forming multiple lower surface expansion structures in electrical

communication with the bottom electrode by:
forming gaps between the at least one lower surface expansion structures;
exposing sidewalls of the lower surface expansion structures and portions of the bottom electrode;
conformally depositing an insulator film on the portions of the bottom electrode and sidewalls of the multiple lower surface expansion structures; and
forming multiple upper surface expansion structures of the at least one upper surface expansion structure protruding into the gaps and separated from the multiple lower surface expansion structures by the insulator film.

[c5] 5.The method of claim 4, wherein the multiple lower surface expansion structures are interleaved with the multiple upper surface expansion structures.

[c6] 6.The method of claim 1, wherein the at least one lower surface expansion structure is a first spiral shape and the at least one upper surface expansion structure is a second spiral shape configured to be interleaved with the first spiral shape.

[c7] 7.The method of claim 1, further comprising fabricating a second capacitor using the steps of claim 1, and arranging the second capacitor on a top of the capacitor of claim 1.

[c8] 8.The method of claim 1, further comprising:
forming a bottom electrode;
forming at least one lower surface expansion structure to the bottom electrode;
conformally depositing an insulator film to exposed portions of the bottom electrode and at least one lower surface expansion structure;
forming a top electrode without at least one upper surface expansion structure separated from the at least one lower surface expansion structure by the insulator film.

[c9] 9.The method of claim 1, wherein the top electrode and the at least one upper surface expansion structures are formed simultaneously.

[c10] 10.The method of claim 1, wherein the at least one lower surface expansion structure is formed by:
depositing an interlayer dielectric material on the bottom electrode;
patterning the interlayer dielectric material to form factors;
depositing conductor material into the features such that the conductor material is in content with the bottom electrode;
further patterning the interlayer dielectric material to form gaps between the deposited conductor material.

[c11] 11.The method of claim 10, wherein the patterning of the interlayer dielectric layer is one of dual tone resist, sidewall image transfer and masking using self-assembled nanocrystals.

[c12] 12.A capacitor, comprising:
at least one lower surface expansion structure having a unit repeatable segment;
an insulator film conformally disposed on a surface of the at least one lower surface expansion structure;
at least one upper surface expansion structure disposed adjacent the insulator film and having a unit repeatable segment interleaved with the unit repeatable segment of at least one lower surface expansion structure; and
a lower electrical contact in electrical communication with the at least one lower surface expansion structure, and an upper electrical contact in electrical communication with the at least one upper surface expansion structure.

[c13] 13.The capacitor of claim 12, wherein the at least one lower surface expansion structure is capacitively coupled to the at least one upper surface expansion structure mostly in a vertical dimension.

[c14] 14.The capacitor of claim 13, wherein the at least one

lower surface expansion structure and the upper surface expansion structure is multiple lower surface expansion structures and multiple upper surface expansion structures having unit repeatable segments interleaved with one another and separated from one another by the conformally disposed insulator film.

[c15] 15.The capacitor of claim 12, wherein the aspect ratio of the at least one lower and upper surface expansion structure is greater than 1.

[c16] 16.The capacitor of claim 12, wherein the unit repeatable segment of the at least one lower surface expansion structure comprises a first spiral shaped surface expansion structure and the unit repeatable segment of the at least one upper surface expansion structure comprises a second spiral shaped surface expansion structure configured to be interleaved with the first spiral shaped surface expanding structure at least one lower surface expansion structure.

[c17] 17.A capacitor, comprising:
a bottom electrode;
a lower electrode fin disposed on the bottom electrode defining a first spiral shape having concentric layers;
an upper electrode;
an upper electrode fin coupled to the upper electrode

and defining a second spiral shape having concentric layers, the concentric layers of the upper electrode fin are configured to interleave between the concentric layers of the lower electrode fin; and
an insulator film conformally disposed between the lower and upper electrode fins.

[c18] 18.The capacitor of claim 17, wherein the capacitor is divided into sections wherein each section comprises a known capacitance and each section comprises a length of a spiral electrode.

[c19] 19.The capacitor of claim 18, configured to have its capacitance value adjusted by changing a number of sections of known capacitance.

[c20] 20.The capacitor of claim 17, wherein one of a height of the lower and upper electrode fin is greater than a respective thickness of the lower and upper electrode fin and a height of the lower and upper electrode fin is at least twice a respective thickness of the lower and upper electrode fin.

[c21] 21.The capacitor of claim 17, further comprising a conductive ring surrounding the lower electrode fin and in electrical contact with the bottom electrode.